Doc. version :	0.2
Total pages :	39
Date :	2005 / 11 / 15

Product Specifications

1.5” COLOR LPTS TFT-LCD MODULE

MODEL NAME: A015BL02 V3
(Green Product, RoHS Compliance)

<◆>Preliminary Specifications

< > Final Specifications

Note: The content of the specifications is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2005/07/08		Draft
0.1	2005/09/12	33~34 38~39	Update Typical Application Circuit Update Recommend Serial Command Setting
0.2	2005/11/15	2 26 29 33	Physical Specifications Optical specification Modify outline dimension Modify PWM efficiency

Contents:

A. Physical Specifications

NO.	Item	Specification	Remark
1	Display resolution(dot)	502(W) × 240(H)	
2	Active area(mm)	30.62(W) × 22.8(H)	
3	Screen size(inch)	1.5 (Diagonal)	
4	Dot pitch(mm)	0.061(W) × 0.095(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	37.1(W) × 32.8(H) × 2.9(D)	Note 1
7	Weight(g)	6.6	
8	Panel Surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 7

B. Electrical specifications

1. Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	CS	I	Serial command enable signal	**Note 1**
2	SDA	I	Serial command data input	**Note 1**
3	SCL	I	Serial command clock input	**Note 1**
4	HSYNC	I	Horizontal sync input	
5	VSYNC	I	Vertical sync input	
6	DCLK	I	Input data clock	
7	D7	I	Data input; MSB	
8	D6	I	Data input	
9	D5	I	Data input	
10	D4	I	Data input	
11	D3	I	Data input	
12	D2	I	Data input	
13	D1	I	Data input	
14	D0	I	Data input; LSB	
15	DRV	O	VLED boost transistor driving signal	
16	VLED	P	LED power: anode	
17	FB	I / P	LED power: cathode	
18	AVDD	C	Power setting capacitor	
19	AGND	P	Ground for analog circuit	
20	GND	P	Ground for digital circuit	
21	VCC	P	Power supply for integrated LCD driver IC	
22	V1	C	Power setting capacitor	
23	V2	C	Power setting capacitor	
24	V3	C	Power setting capacitor	
25	V4	C	Power setting capacitor	
26	V5	C	Power setting capacitor	
27	V6	C	Power setting capacitor	

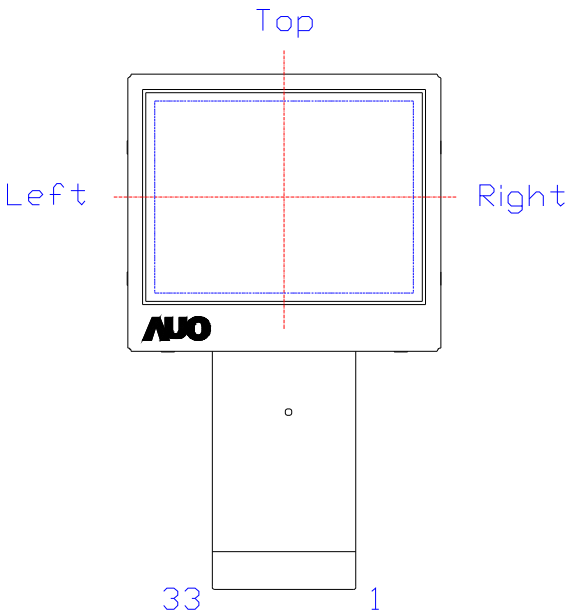
28	V7	C	Power setting capacitor	
29	V8	C	Power setting capacitor	
30	FRP	O	VCOM driving signal	Note 2
31	VGL	C	Power setting capacitor	
32	VGH	C	Power setting capacitor	
33	VCOM	I	Common voltage	

I: Input; O: Output; P: Power; C: Capacitor.

Note 1: 3-wire serial control interface is operational after VCC power on reset, but execution of programmed commands is synchronized at front edge of next VSYNC pulse.

Note 2: FRP is the output of Vcom driver. It is the same phase and amplitude with common electrode driving signal (Vcom). The Vcom amplitude and DC level setting can be adjusted through serial control. External Vcom DC adjustment is also achievable. Please refer to the application note for details.

Note 3: For pin sequence arrangement and scan direction, please refer to the figure as below:



2. Absolute maximum ratings

Stresses beyond those given in the Absolute Maximum rating table may cause operational error or damage to the device.

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Driver IC Power Voltage	VCC	AGND = GND = 0V	-0.3	+4.5	V	
TFT-LCD Power Voltage	VGH	AGND = GND = 0V	-0.3	+10	V	
	VGL	AGND = GND = 0V	-7	+0.3	V	
Input Signal Voltage	CS, SDA, SCL, HSYNC, VSYNC, DCLK, D0~D7	AGND = GND = 0V	-0.3	VCC+0.5	V	
VCOM AC Output Voltage	FRP	AGND = GND = 0V	-0.3	+8	V	
VCOM Input Voltage	VCOM	AGND = GND = 0V	-0.3	+10	V	
Charge Pump Voltage	AVDD	AGND = GND = 0V	-0.3	+7	V	
	V1	AGND = GND = 0V	-0.3	+7	V	
	V2	AGND = GND = 0V	-0.3	+7	V	
	V3	AGND = GND = 0V	-0.3	+10	V	
	V4	AGND = GND = 0V	-0.3	+7	V	
	V5	AGND = GND = 0V	-0.3	+7	V	
	V6	AGND = GND = 0V	-7	+0.3	V	
	V7	AGND = GND = 0V	-0.3	+7	V	
	V8	AGND = GND = 0V	-7	+0.3	V	
PWM Control Signals	DRV	AGND = GND = 0V	-0.3	VCC+0.3	V	
	FB	AGND = GND = 0V	-0.3	VCC+0.3	V	
Operating temperature	Topa		0	60	℃	Ambient temperature
Storage temperature	Tstg	-	-25	80	℃	Ambient temperature

3. Electrical Specifications

a. Power Supply

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage	V_{CC}	GND=AGND=0V	3.15	3.3	3.45	V	Note 1
Power Supply Current	I_{CC}	V_{CC}=3.3V	-	-	19	mA	Note 2
	$I_{CC(STANDBY)}$	V_{CC}=3.3V	-	0.1	-	mA	

Note 1: A build-in power on reset circuit for V_{CC} is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after V_{CC} power on through serial command. Please refer to the register STB setting for detail.

Note 2: Test condition: UPS052 320X240 mode, DCLK = 27MHz, black pattern.

b. Input / Output Signal Voltage (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Signal high level voltage	V_{IH}	—	0.7×V_{CC}	—	—	V	Note 1
Input Signal low level voltage	V_{IL}	—	—	—	0.3×V_{CC}	V	
TFT-LCD Power Voltage	V_{GH}	V_{CC}=3.3V	8.5	9.0	9.5	V	Note 2
	V_{GL}	V_{CC}=3.3V	-7.0	-6.5	-6.0	V	
VCOM AC Output Voltage	V_{CAC}	V_{CC}=3.3V R0=00h	4.8	5.0	5.2	Vp-p	Note 3
		V_{CC}=3.3V R0=03h	5.38	5.6	5.82		
		V_{CC}=3.3V R0=07h	6.14	6.4	6.66		
VCOM DC Output Voltage	V_{CDC}	V_{CC}=3.3V	1.02	1.17	1.32	V	Note 4
DRV output voltage V_{DRV}	V_{DRV}	—	0	-	VCC		
DRV output current	I_{DRV}	—	-	0.2	10		Note 5
Feedback voltage V_{FB}	V_{FB}	—	0.57	0.6	0.63		

Note 1: Applicable pins: CS, SDA, SCL, VSYNC, HSYNC, DCLK, D0~D7

Note 2: V_{GH} and V_{GL} are output voltages of integrated power generation circuit.

Note 3: The amplitude of V_{CAC} could be adjusted to change the brightness of LCD panel. Applicable pins: VCOM, FRP.

Note 4: The V_{CDC} could be adjusted to minimize flicker and maximize contrast on each LCD panel. Applicable pins: VCDC

Note 5: I_{DRV} (typ.) based on the recommend application circuit

c. Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
AVDD	4.7	10 or more
VGH	4.7	10 or more
VGL	4.7	10 or more
V1(+), V2(-)	2	10 or more
V3(-), V4(+)	2	10 or more
V5(+), V6(-)	2	10 or more
V7(-), V8(+)	2	10 or more

c. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_L	-	20	30	mA	
LED voltage	V_L	-	4.2	4.6	V	
LED Life Time	T_L	10000	-	-	Hr	Note 1,2

Note 1: Typical voltage:3.6V/pcs ,FB=0.6V. LED voltage: VLED=3.6+0.6=4.2V

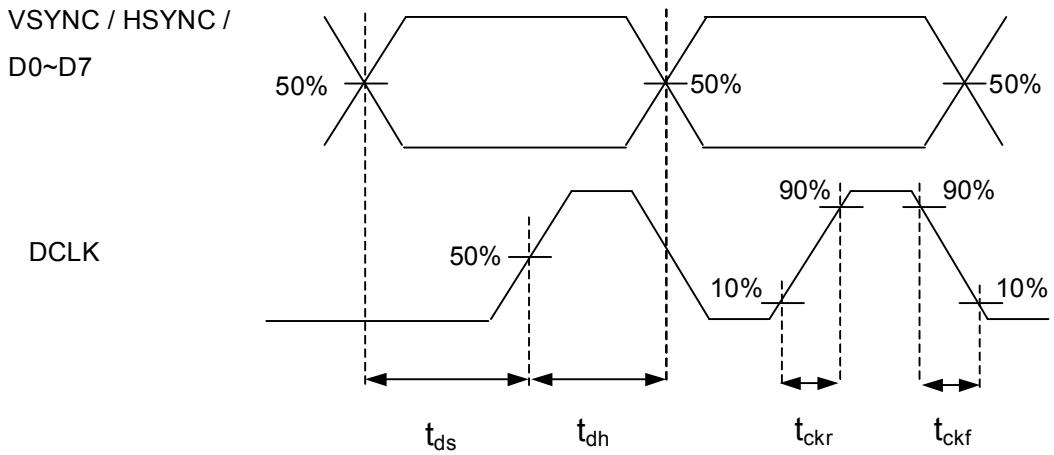
Please refer to Fig.13 (P.34)

Note 2 : Ta. = 25℃, I_L = 20mA

Note 3 : Brightness to be decreased to 50% of the initial value.

4. AC Timing

a. Input Signal Setup Time / Hold Time



Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Input Signal Setup Time	t_{ds}	6	—	—	nsec	
Input Signal Hold Time	t_{dh}	6	—	—	nsec	
Clock Rising Time	t_{ckr}	0	—	10	nsec	
Clock Falling Time	t_{ckf}	0	—	10	nsec	

b. UPS051 timing specifications (refer to Fig. 1, Fig. 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	9.17(*)	13.5	13.59	MHz	
HSYNC	Period	t_H	624	858	864	t_{DCLK}	Note 1
	Display period	t_{hdisp}	502			t_{DCLK}	
	Blanking	t_{hblk}	22	30	255	t_{DCLK}	
	Front porch	t_{hfp}	100	326	—	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hblk} -1	t_{DCLK}	
VSYNC	Period	t_V	245	262.5	265	t_H	Note 2
	Display period	t_{vdisp}	240			t_H	
	Blanking	t_{vblk}	3	21	31	t_H	
	Pulse width	t_{vsw}	1	1	t_{vblk} –1	t_{DCLK}	
Data set-up time		t_{ds}	12	—	—	ns	
Data hold time		t_{dh}	12	—	—	ns	
Vsync-to-Hsync set-up time		t_{vhs}	1	—	—	t_{DCLK}	

(*) when t_V =245 t_H

Note 1: UPS051 Horizontal blanking time (t_{hblk}) is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical blanking time (t_{vblk}) is adjustable by setting register VBLK. UPS051 accepts odd-field-only or even-field-only vertical input format.

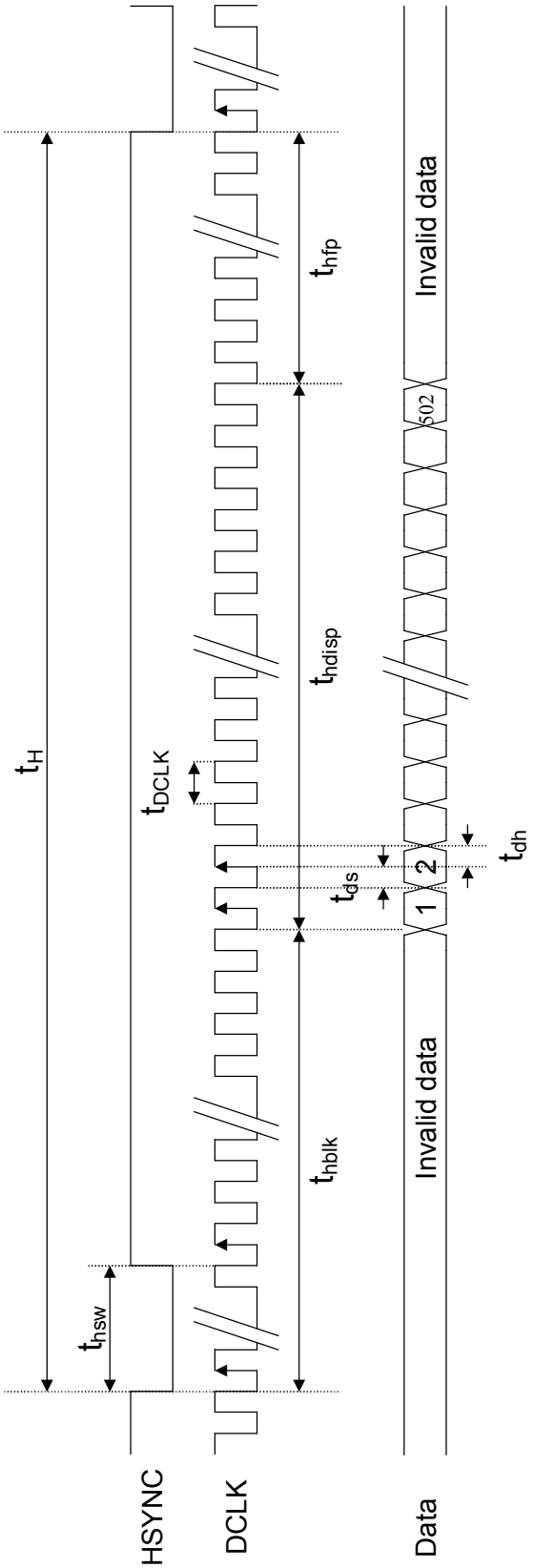


Fig.1 UPS051 Input Horizontal Signal

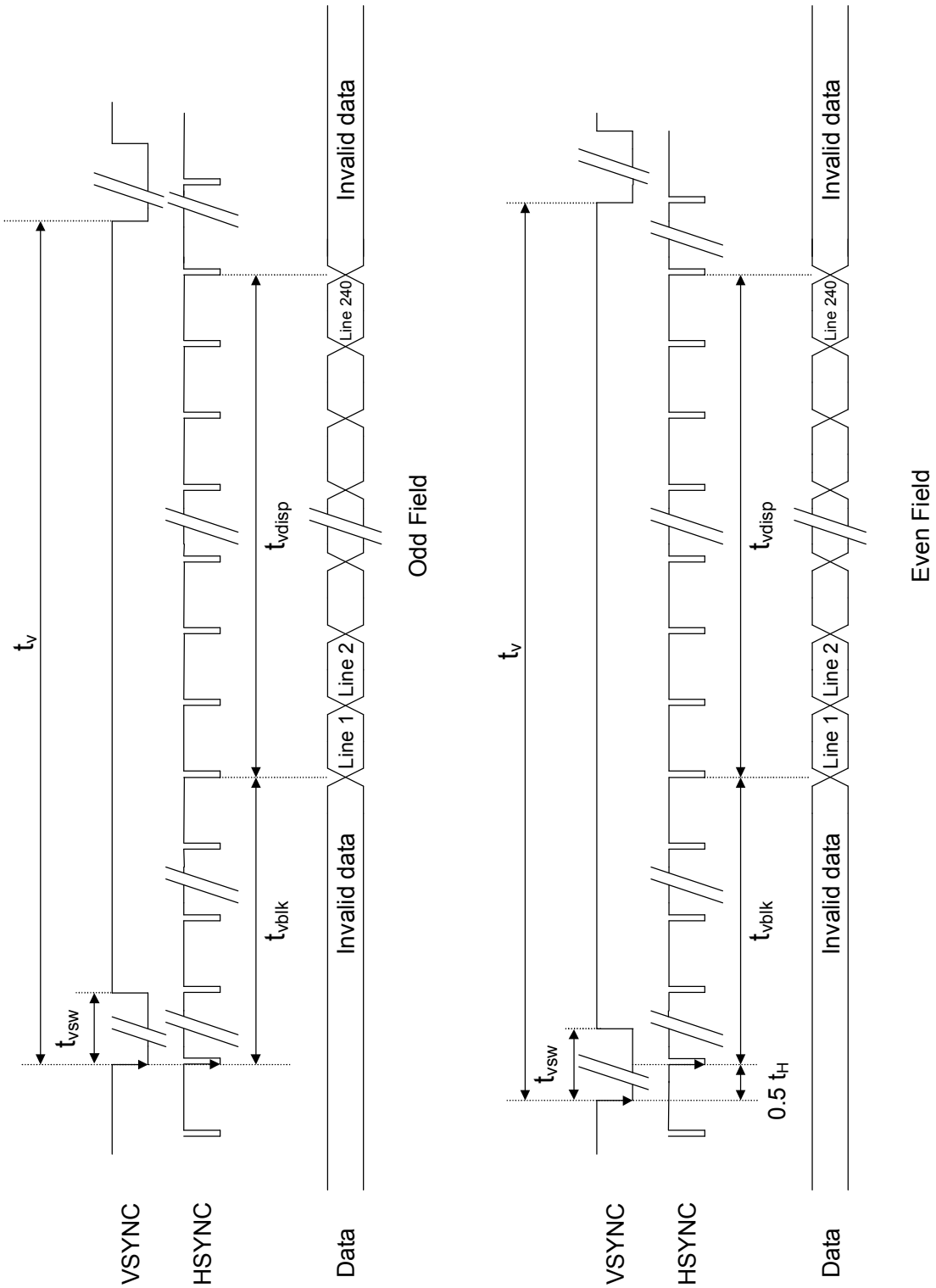


Fig.2 UPS051 Input Vertical Signal

c – 1. UPS052 (320 mode/NTSC/24.545MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		24.545		MHz	
HSYNC	Period	t_H		1560		t_{DCLK}	
	Display period	t_{hdisp}		1280		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		262.5		t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

c - 2. UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		24.375		MHz	
HSYNC	Period	t_H		1560		t_{DCLK}	
	Display period	t_{hdisp}		1280		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		312.5		t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

d - 1. UPS052 (352 mode/NTSC/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1716		t_{DCLK}	
	Display period	t_{hdisp}		1408		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		262.5		t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

d - 2. UPS052 (352 mode/PAL/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1728		t_{DCLK}	
	Display period	t_{hdisp}		1408		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		312.5		t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

e - 1. UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1716		t_{DCLK}	
	Display period	t_{hdisp}		1440		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		262.5		t_H	
	Display period	t_{vdisp}		240		t_H	
	Blanking	t_{vblk}		21		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

e - 2. UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig. 3, Fig. 4)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		27		MHz	
HSYNC	Period	t_H		1728		t_{DCLK}	
	Display period	t_{hdisp}		1440		t_{DCLK}	
	Blanking	t_{hblk}		241		t_{DCLK}	
	Pulse width	t_{hsw}		1		t_{DCLK}	
VSYNC	Period	t_V		312.5		t_H	
	Display period	t_{vdisp}		288		t_H	
	Blanking	t_{vbp}		24		t_H	
	Pulse width	t_{vsw}		1		t_{DCLK}	

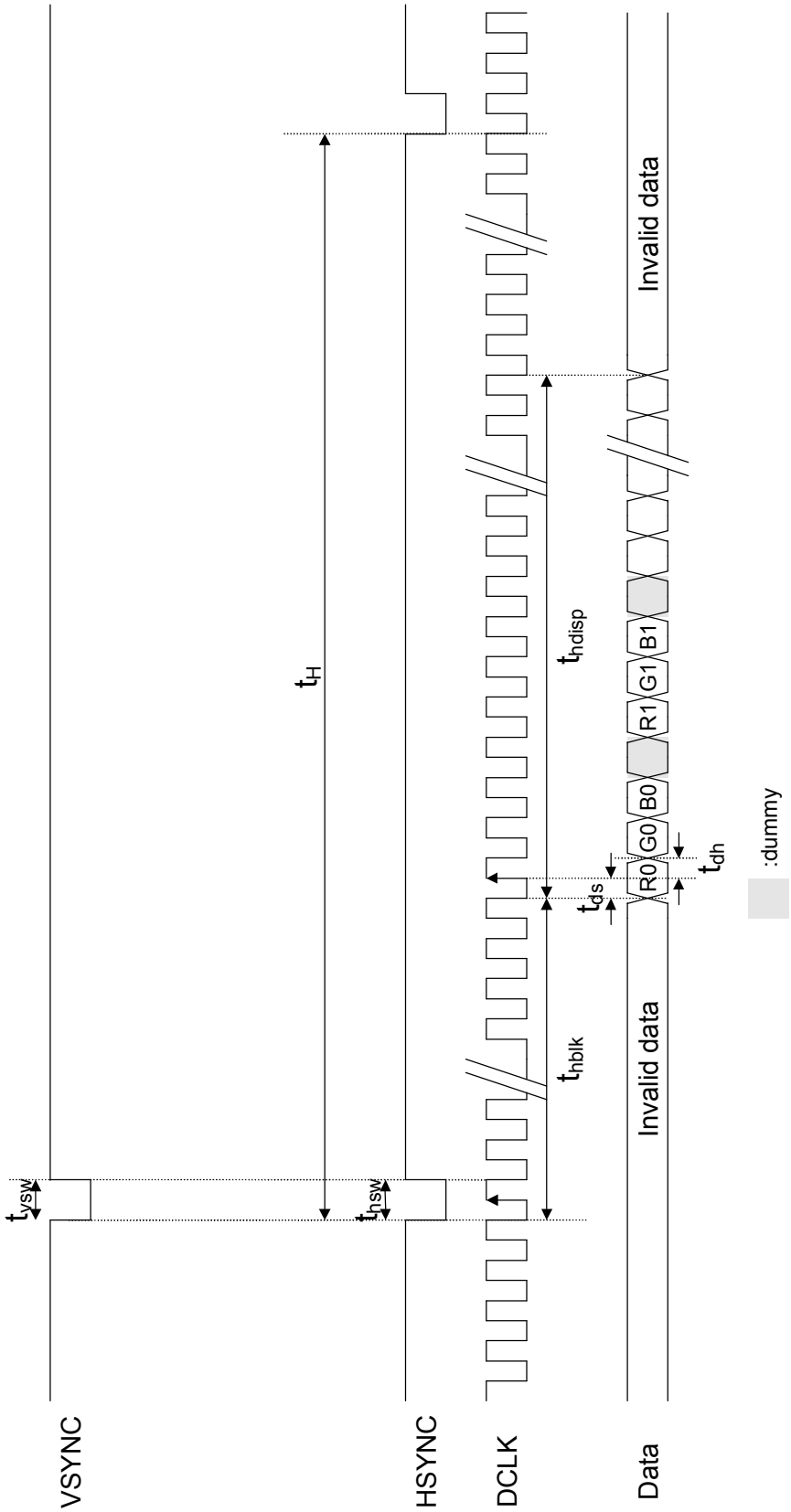


Fig. 3 UPS052 Input Horizontal Signal

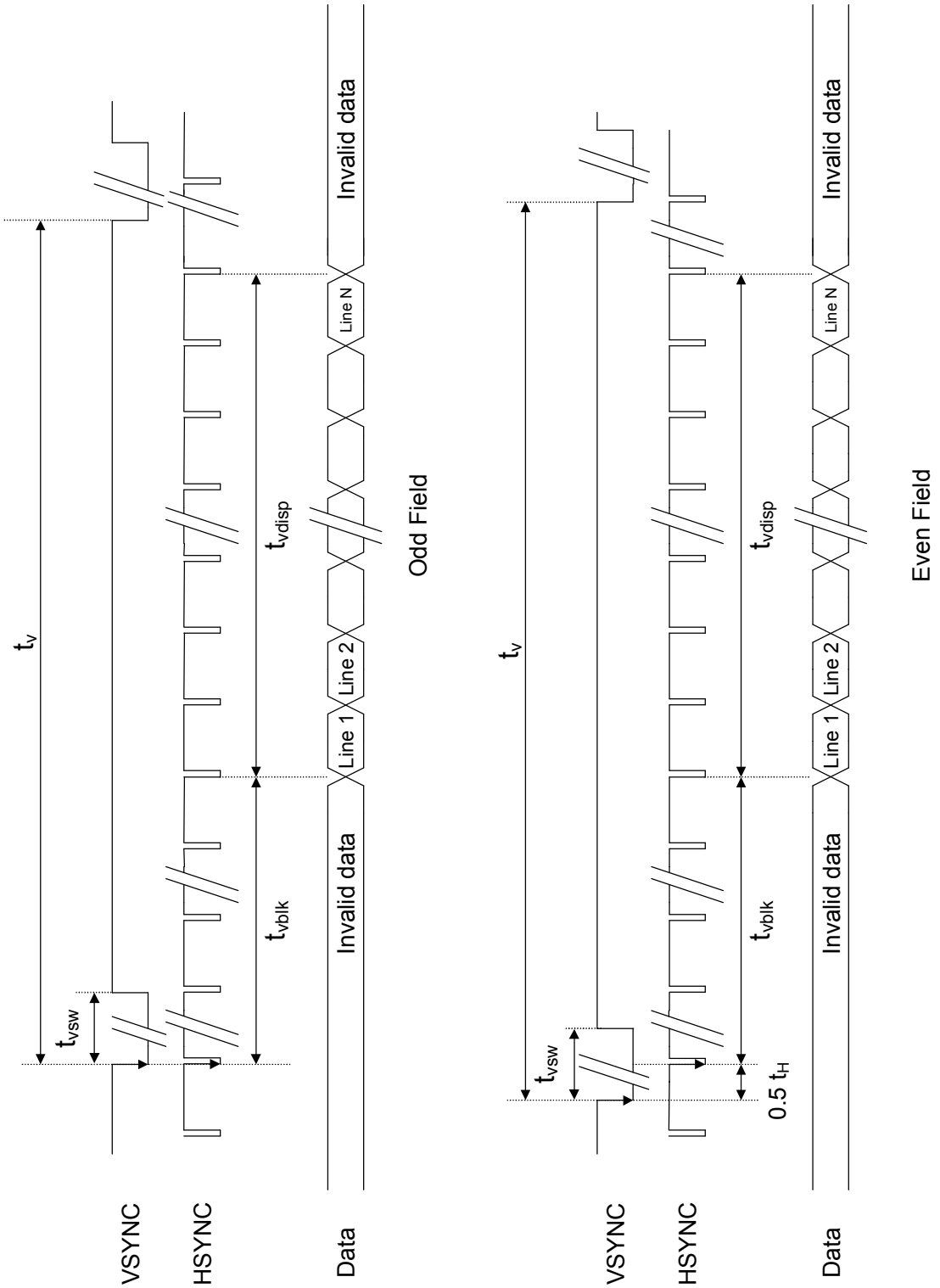


Fig.4 UPS052 Input Vertical Signal

f -1. CCIR656 Timing chart

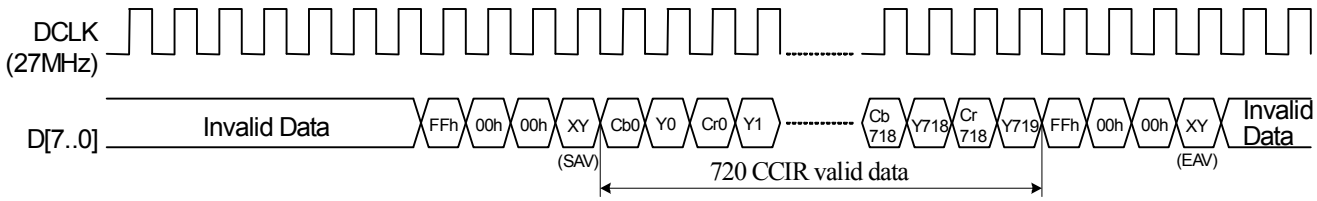


Fig. 5: CCIR656 Data input format

f –2. CCIR656 decoding

FF 00 00 XY signals are involved with HSYNC,VSYNC and Field

XY encode following bits:

F=field select

V=indicate vertical blanking

H=1 if EAV else 0 for SAV

P3-P0=protection bits

P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H

⊕represents the exclusive-OR function.

Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.

Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0

f – 3.CCIR656 to RGB conversion

R=Y +1.371*(Cr-128)

G=Y -0.698(Cr-128)-0.336(Cb-128)

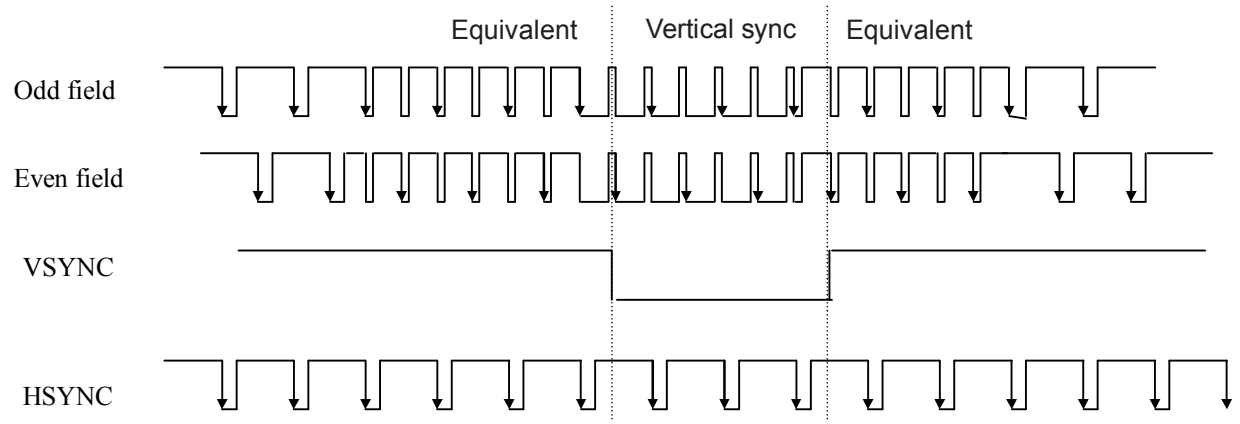
B=Y +1.732(Cb-128)

Where Y:16~235 Cr:16~240 Cb:16~240

In CCIR656 mode , please set series command **R3=2Eh & R13=4Bh** for the better contrast .

g. CSYNC Timing chart

NTSC mode



PAL mode

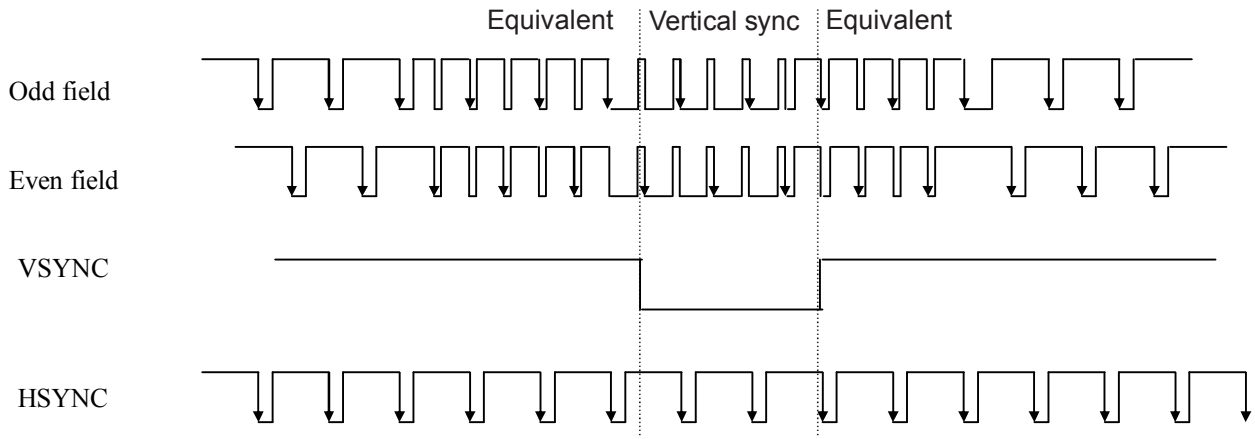


Fig. 6: CSYNC Data input format

Item	Min	Typ	Max
HYSNC width	2 clk	4.7us	6us
Equivalent pulse width	1 clk	2.35us	3us
Serrated pulse width (inside VSYNC)	2 clk	4.7us	6us
VSYNC width	2.3H	NTSC:3H PAL:2.5H	10H

5. Serial Control Interface

a. Input timing specifications (refer to Fig. 7)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial load input setup time	t_{s0}	50	—	—	ns	
Serial load input hold time	t_{h0}	50	—	—	ns	
Serial data input setup time	t_{s1}	50	—	—	ns	
Serial data input hold time	t_{h1}	50	—	—	ns	
SCL pulse width	t_{w1L}	100	—	—	ns	
	t_{w1H}	100	—	—	ns	
CS pulse width	t_{W2}	400	—	—	ns	

b. Serial setting map

No	Register Address								Register Data (Default setting)							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	×	×	×	0	0	0	0	0	×	×	×	×	×	VCOM_AC (011)		
R1	×	×	×	0	0	0	0	1	×	FLK (0)	VCOM_DC (18h)					
R3	×	×	×	0	0	0	1	1	BRIGHT (40h)							
R4	×	×	×	0	0	1	0	0	×	YUV(0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	×	×	×	0	0	1	0	1	×	GRB (1)	PWMM (1)	PWM_DUTY (10)		SHDB2 (1)	SHDB1 (1)	STB (0)
R6	×	×	×	0	0	1	1	0	×	LED_CURRENT (00)		VBLK (15h)				
R7	×	×	×	0	0	1	1	1	HBLK (1Eh)							
R8	×	×	×	0	1	0	0	0	×	×	×	×	D_SAMP (0)	PSL (000)		
R12	×	×	×	0	1	1	0	0	×	×	CSYNC (1)	CbCr (0)	×	Vdpol (1)	Hdpol (1)	DCLK pol (0)
R13	×	×	×	0	1	1	0	1	CONTRAST(40h)							
R14	×	×	×	0	1	1	1	0	×	SUB-CONTRAST_R(40h)						
R15	×	×	×	0	1	1	1	1	×	SUB-BRIGHTNESS_R(40h)						
R16	×	×	×	1	0	0	0	0	×	SUB-CONTRAST_B(40h)						
R17	×	×	×	1	0	0	0	1	×	SUB-BRIGHTNESS_B(40h)						
R18	×	×	×	1	0	0	1	0	Gamma_VR2(8h)				Gamma_VR1(8h)			
R19	×	×	×	1	0	0	1	1	Gamma_VR4(8h)				Gamma_VR3(8h)			

× : Dummy bit ,please set to '0'

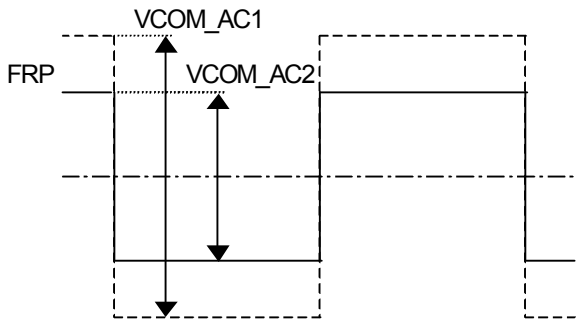
c. Description of Serial Control Operations

- ●Each serial command consists of 16 bits of data, which is loaded one bit a time at the rising edge of serial clock SCL.
- ●Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- ●The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
- ●If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- ●If 16 bits or more of SCL are input while CS is low, the last 16 bits of transferred data before the rising edge of CS pulse are valid data.
- ●Serial block operates with the SCL clock
- ●Serial data can be accepted in the power save mode.

d. Description of serial control data

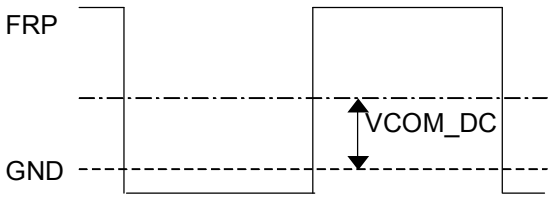
(1) VCOM_AC: Common voltage AC level selection; 3 bit setting, 0.2V / LSB (deviation ±4%)

(MSB – LSB)	VCOM AC LEVEL	UNIT
000	5.0	V
001	5.2	
010	5.4	
011	5.6 (Default)	
100	5.8	
101	6.0	
110	6.2	
111	6.4	



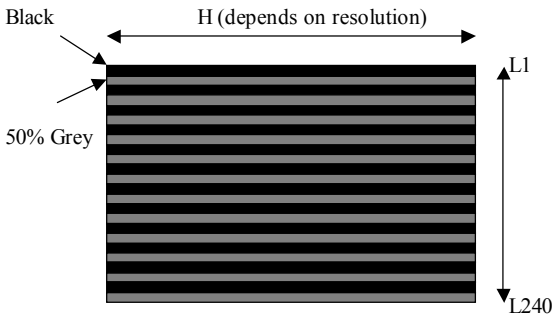
(2) VCOM_DC : Common voltage DC level selection; 6 bit setting, 27mV / LSB

(MSB – LSB)	VCOM AC LEVEL	UNIT
00h	1.75	V
18h	1.1(Default)	
3Fh	0	



(3) FLK : flicker pattern output

FLK	Function
0	Normal operation (Default)
1	Flicker patttern output



(4) BRIGHTNESS : RGB bright level setting; 8-bit setting

(MSB-LSB)	Function
00h	Dark
40h	Center (Default)
FFh	Bright

(5) HDIR : Horizontal scan direction setting

HDIR	Function
0	Right-to-left scan
1	Left-to-right scan (Default)

(6) VDIR : Vertical scan direction setting

VDIR	Function
0	Down-to-up scan
1	Up-to-down scan (Default)

(7) NTSC/PAL : NTSC or PAL mode selection (for UPS052 input timing)

(MSB-LSB)	Function
00	PAL mode
01	NTSC mode
10	Auto-detection mode (Default)
11	

(8) SEL : Input data timing format selection; please refer to AC timing section for detail specifications.

(MSB-LSB)	Input Timing Format
00	UPS051 (Default)
01	UPS052: 320x240
10	UPS052: 352x240
11	UPS052: 360x240

(9) YUV : :YUV(CCIR656) or RGB input selection

YUV	Function
0	RGB input (Default)
1	YUV input

Note: If YUV='1' & CSYNC='0' ,YUV is the input signal

(10) STB : Standby (power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

(11) SHDB1: Shut-down of the power boost converter for LED backlight unit

SHDB1	Function
0	The LED power converter is off
1	The LED power converter is controlled by build-in on/off sequence (Default)

(12) SHDB2: Shut-down for VGH/VGL charge pump

SHDB2	Function
0	The VGH/VGL charge pump is off
1	The VGH/VGL charge pump is controlled by build-in on/off sequence (Default)

(13) PWM_DUTY: PWM duty cycle selection for LED backlight power converter (valid when PWMM = 0)

(MSB-LSB)	PWM duty cycle
00	50%
01	60%
10	65% (Default)
11	70%

(14) PWMM: PWM mode selection

PWMM	Function
0	Mode 0: fixed duty cycle
1	Mode 1: increasing duty cycle (Default)

(15) GRB: Register reset setting

GRB	Function
0	Reset all registers to default values
1	Normal operation (Default)

(16) VBLK: Vertical blanking setting for UPS051; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
00h	0	line
15h	21 (Default)	
1Fh	31	

Vertical blanking setting for CCIR656 NTSC mode; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
00h	0	line
16h	22 (Default)	
1Fh	31	

Vertical blanking setting for CCIR656 PAL mode; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
00h	3	line
15h	24 (Default)	
1Fh	34	

Note: When input data timing is set to the CCIR656 mode, V-blanking must be adjusted based on the input data.

(17)LED_CURRENT:adjust LED current

(MSB-LSB)	Feedback threshold voltage
00	0.6V(default,20mA)
01	0.75V(25mA)
10	0.45V(15mA)
11	0.3V(10mA)

(18) HBLK: Horizontal blanking setting for UPS051; 8-bit setting, 1 DCLK/LSB

(MSB-LSB)	H-blanking t_{hblk}	UNIT
00h	0	DCLK
1Eh	30 (Default)	
FFh	255	

(19) PSL : Panel resolution selection

(MSB-LSB)	Function
0XX	Controlled by driver IC input pins : PSL0, PSL1 (Default)
100	502 * 240 (dots)
101	640 * 240 (dots)
110	720 * 240 (dots)
111	960 * 240 (dots)

Note : “X“ is “0” or “1”

(20) D_SAMP : Single pulse or dual pulse selection

S_SAMP	Function
0	Single pulse (Default)
1	Dual pulse

(21) DCLKpol : DCLK polarity selection

DCLKpol	Function
0	Positive polarity(Default)
1	Negative polarity

(22) HDpol : HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity(Default)

(23) VDpol : VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity(Default)

(24) CbCr:Cb & Cr exchange position

CbCr='0'(Default)		Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3
CbCr='1'		Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

(25) CSYNC : Separate SYNC or CSYNC input selection

CSYNC	Function
0	CSYNC input
1	Separate SYNC (Default)

Note: If YUV='1' & CSYNC='0' ,YUV is the input signal(VSYNC need connect to VCC).

(26) CONTRAST : RGB contrast level setting, the gain changes (1/64) / bit

(MSB-LSB)	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

(27) SUB-CONTRAST : RB sub-contrast level setting, the gain changes (1/256) / bit

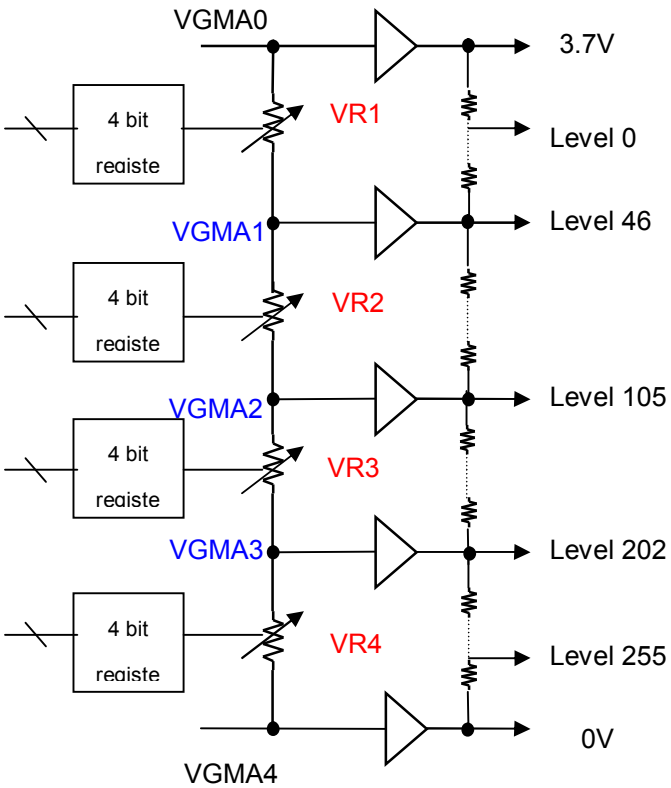
(MSB-LSB)	Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

(28) SUB-BRIGHTNESS : RB sub-bright level setting, setting accuracy: 1 step / bit

(MSB-LSB)	Contrast gain
00h	Dark (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

(29) Gamma_VR1, Gamma_VR2 , Gamma_VR3 , Gamma_VR4 : resistor range 8K(0000)~23K(1111)

(MSB-LSB)	Resistor Value
0000	8K
1000	16K (Default)
1111	23K



1. VGMA1,VGMA2,VGMA3 are generated within driver IC and adjustable through serial register setting
2. VR1,VR2,VR3,VR4 are adjustable through 4 bit registers

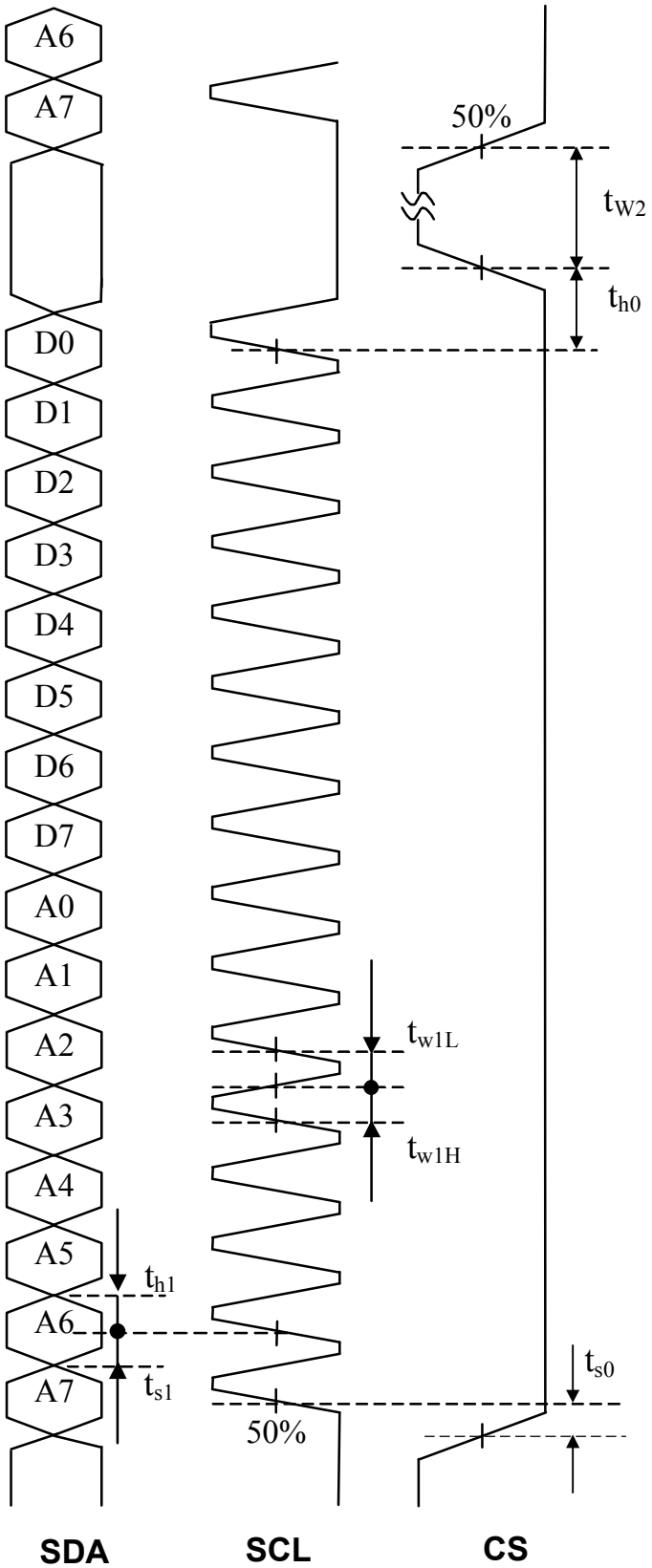


Fig. 7 Serial Control Timing

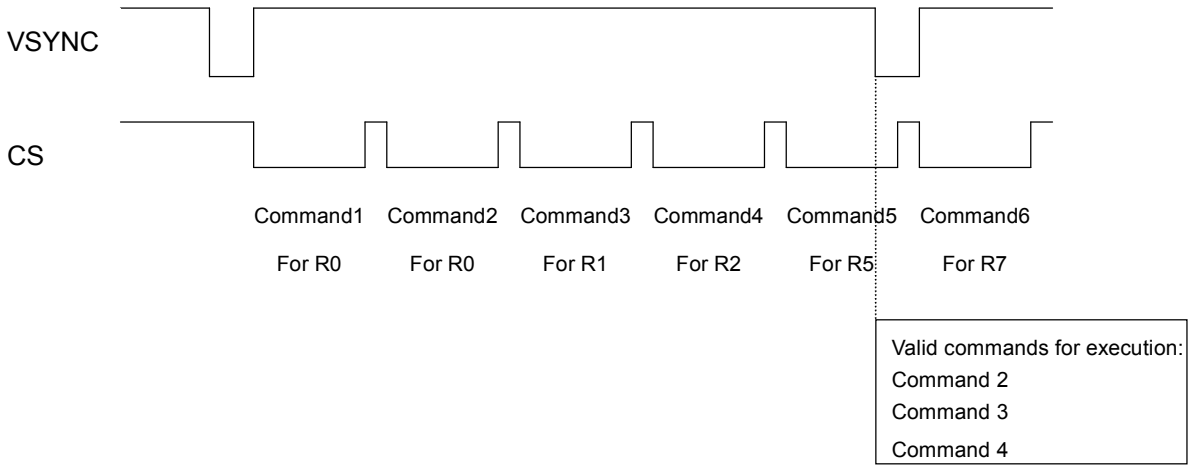


Fig. 8 Example of Serial Command Operation

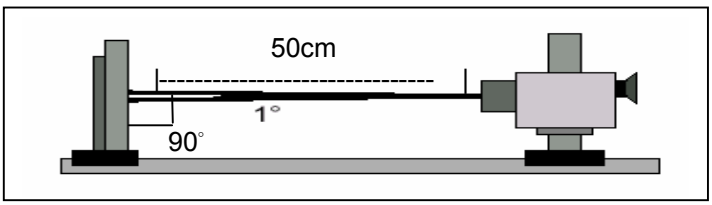
C. Optical specifications (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ =0°	 - -	 15 20	 25 30	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	120	300	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 60 40 40	 20 70 50 50	 -- -- -- --	deg.	Note 7
Brightness	Y_L	θ =0°	150	200		nits	Note 8
White chromaticity	X	θ =0°	0.28	0.33	0.38		
	y	θ =0°	0.30	0.35	0.40		
Backlight Luminance Uniformity			60	75		%	Note 9

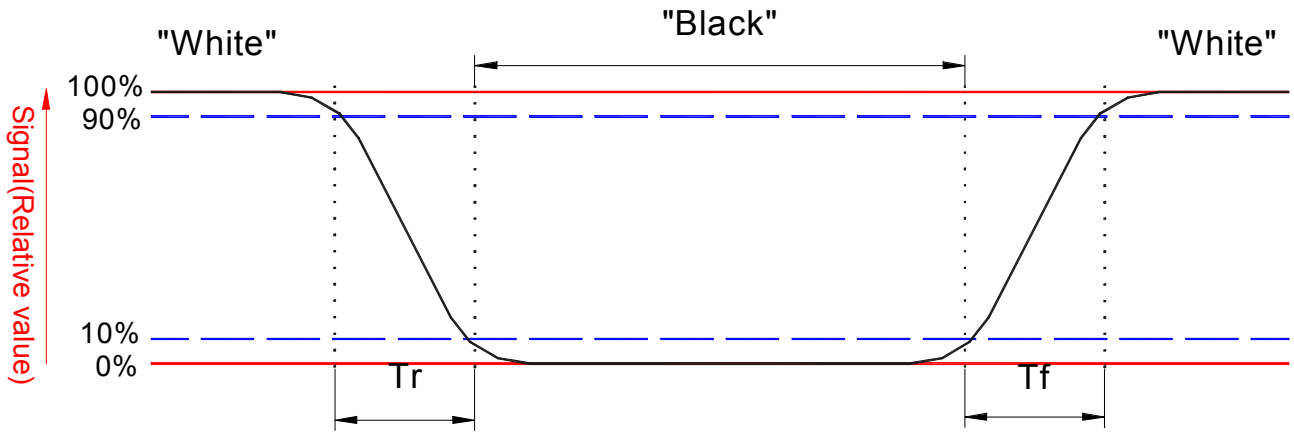
Note 1. Ambient temperature =25℃. And backlight current I_L=20 mA

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation, distance:500±50mm.



Note 4. Definition of response time: The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi=V_{i50} ± 1.5V

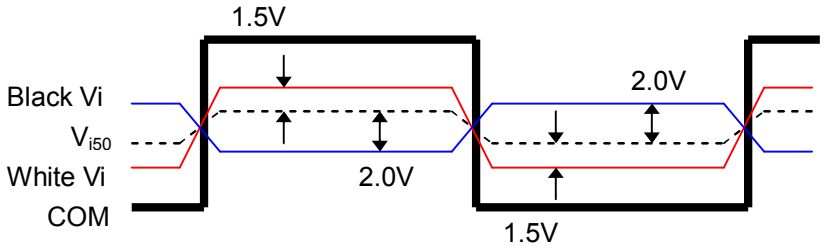
Black Vi=V_{i50} ∓ 2.0V

“±” Means that the analog input signal swings in phase with COM signal.

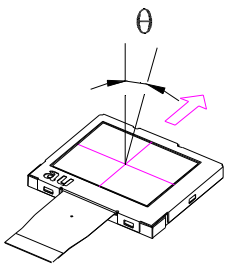
“∓” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

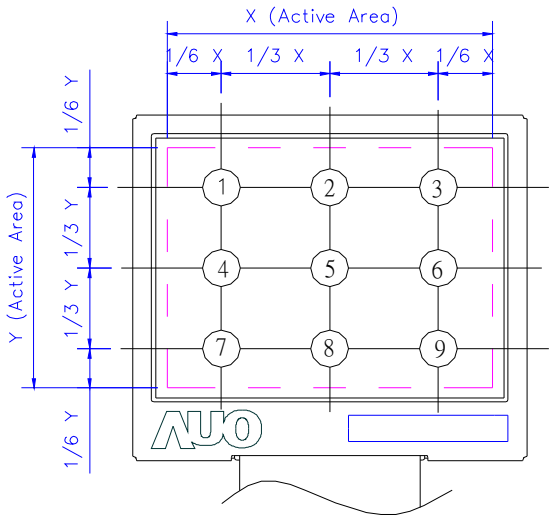


Note 7. Definition of viewing angle:



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9: Definition of luminance uniformity

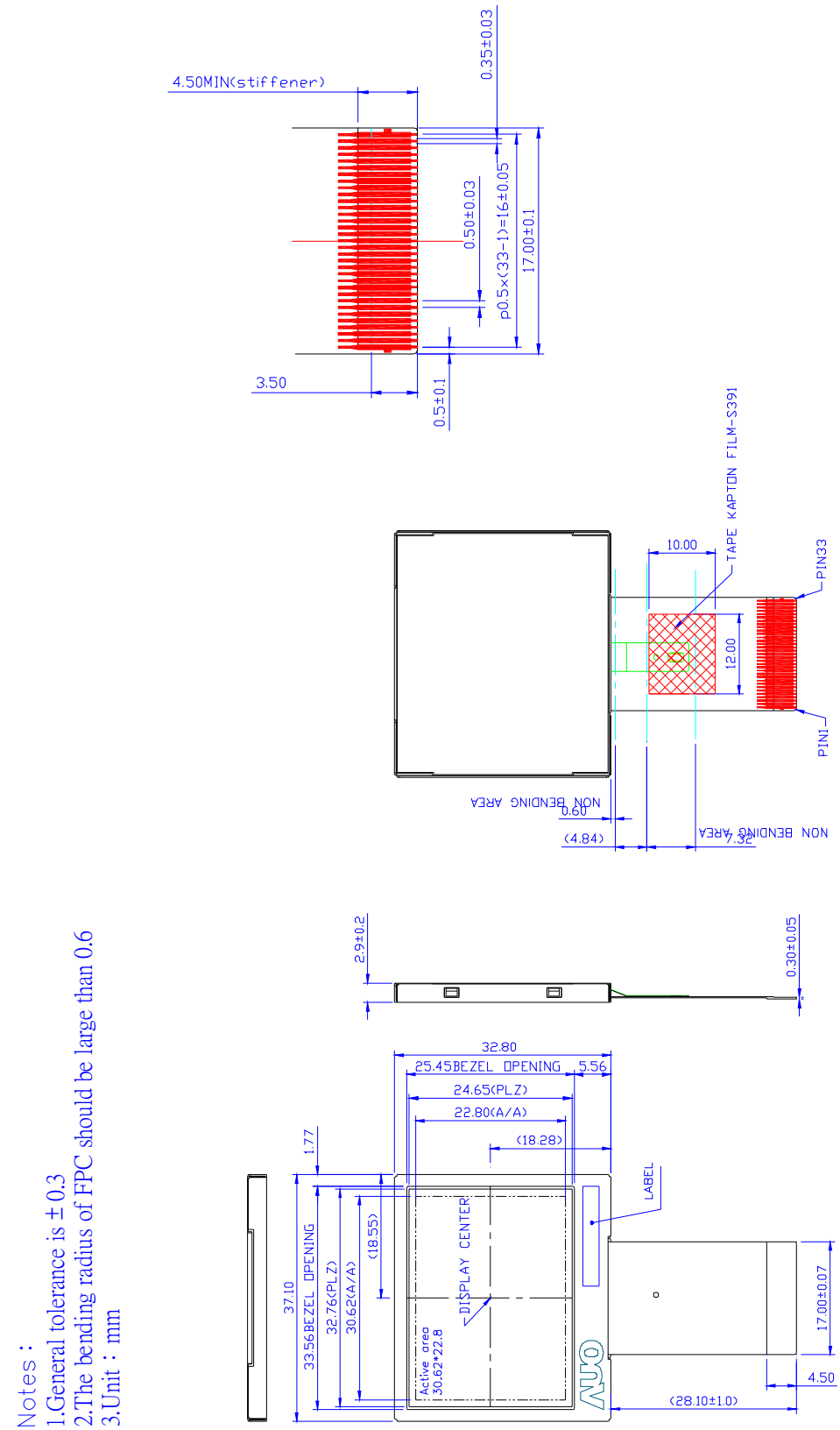


D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

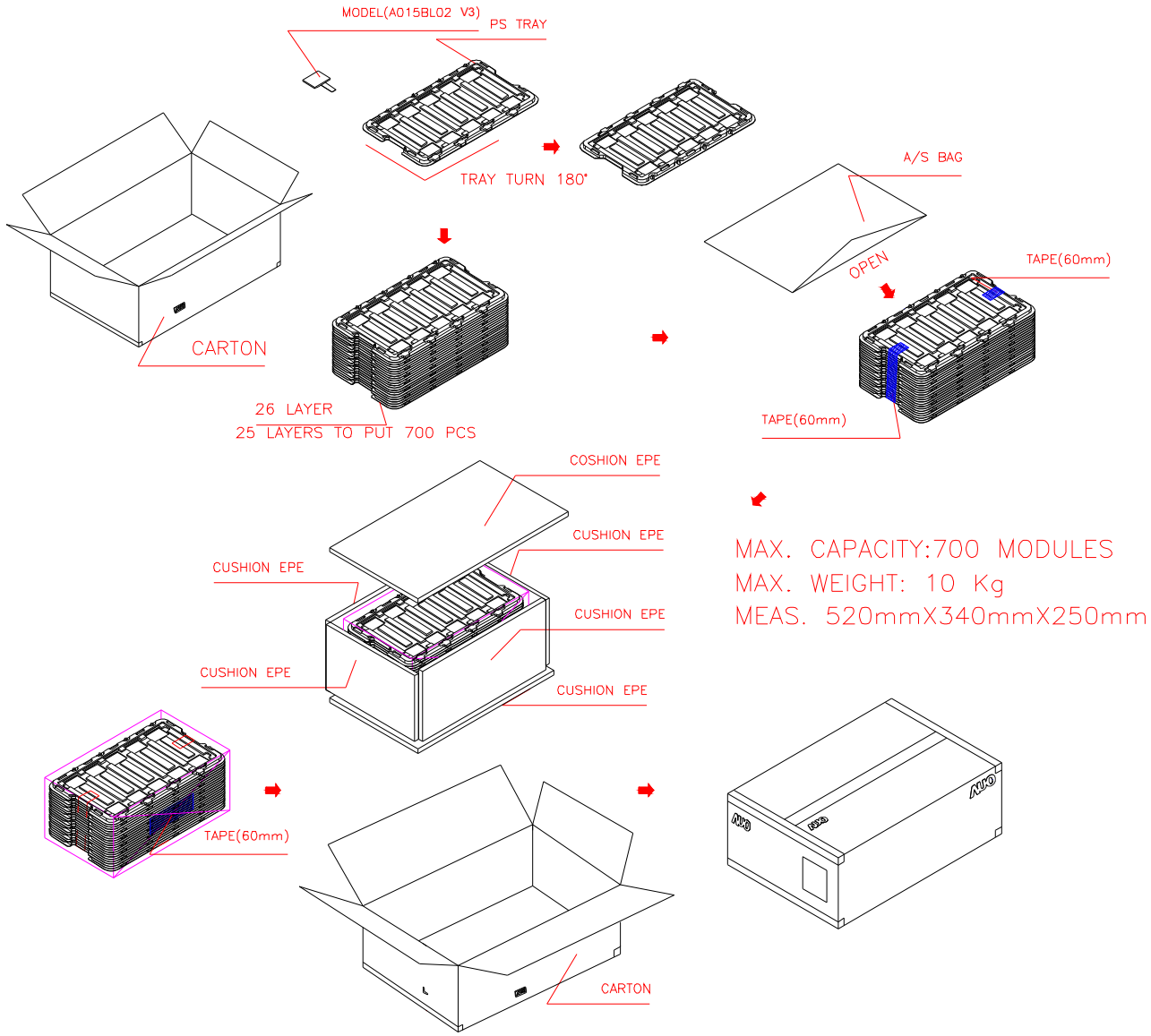
E. Outline dimension



Notes：
1.General tolerance is ± 0.3
2.The bending radius of FPC should be large than 0.6
3.Unit：mm

Fig.9 Outline dimension of TFT-LCD module

F. Packing form



G. Application Notes

This LTPS TFT LCD module is designed for digital still camera application. A COG type LCD driver IC is integrated within this module, makes it much easier to design and cost-effective. The main features of integrated driver are:

- Accepting digital serial R, G, B 8-bit signal, fewer adjustment, fewer design effort, and lower power consumption compared to other analog LTPS solution.
- Integrated timing controller for UPS051 and UPS052 input timing formats. For UPS052 input timing, the input signal is always the same for different panel resolution.
- Integrated LED power converter controller, DC-DC charge pump, and Vcom driver. A design requires less peripheral components and reduces the total system cost.

1. Input Data Timing

Two kinds of input timing format are supported: UPS051 and UPS052. In UPS051 input format, the conversion of image data to display dots is controled by the user. In UPS052 input format, the mapping of incoming data to display dots is take cared by built in scaling function of driver IC.

For UPS051 timing, the module accpet one dot video data at the rising edge of DCLK, and display them one dot by one dot. Therefore the input data timing is different according to different panel resolutions and scan directions. Refer to the AC Timing of UPS051 part, you can use the typ. value for a typical case, or you can use the min. value to lower down the power consumption and EMI.

Because of delta color filter arrangement, the RGB data sequence for even and odd lines are different based on scan direction. For the definition of even and odd lines, see Fig. 10.

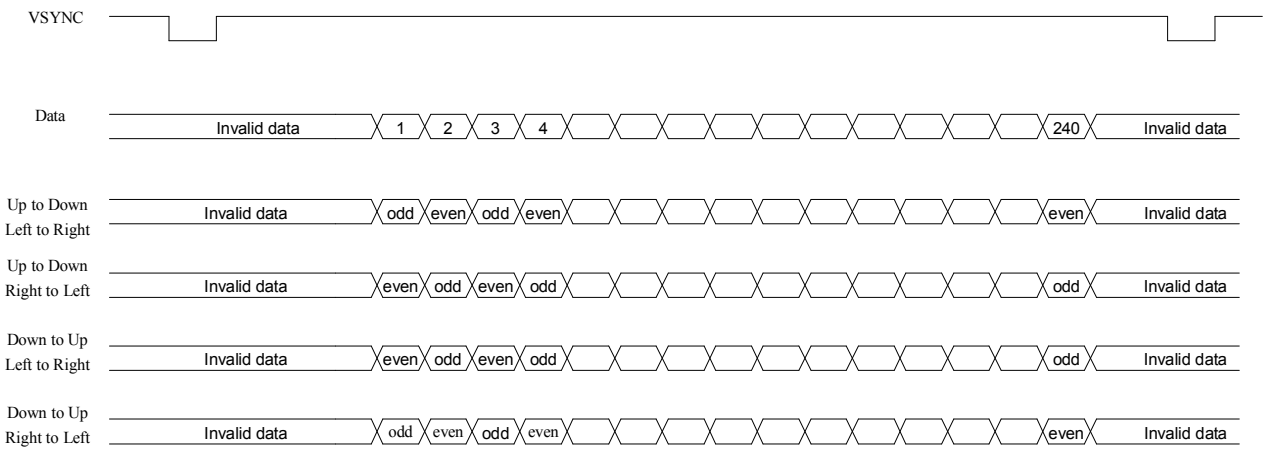


Fig 10. UPS051 even and odd lines definition

For the RGB sequence, see Fig. 11.

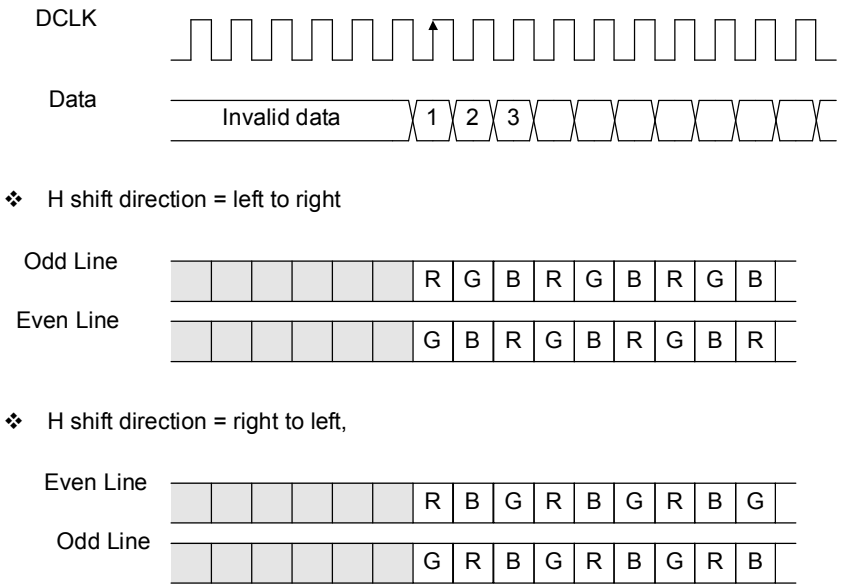


Fig. 11 UPS051 Input RGB sequence

For the color filter arrangement, see Fig. 12.

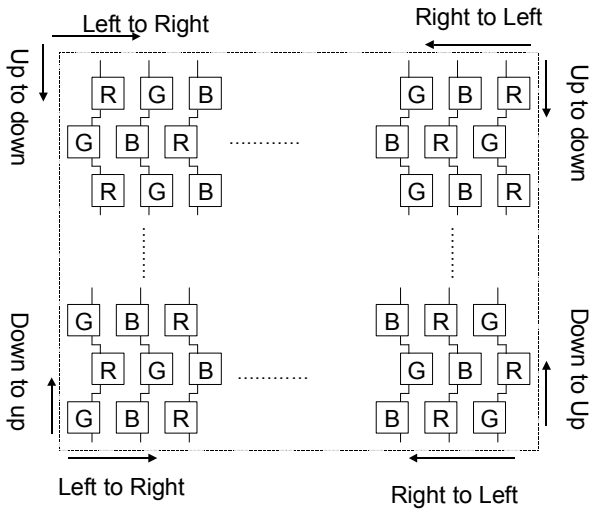


Fig. 12 Color filter arrangement

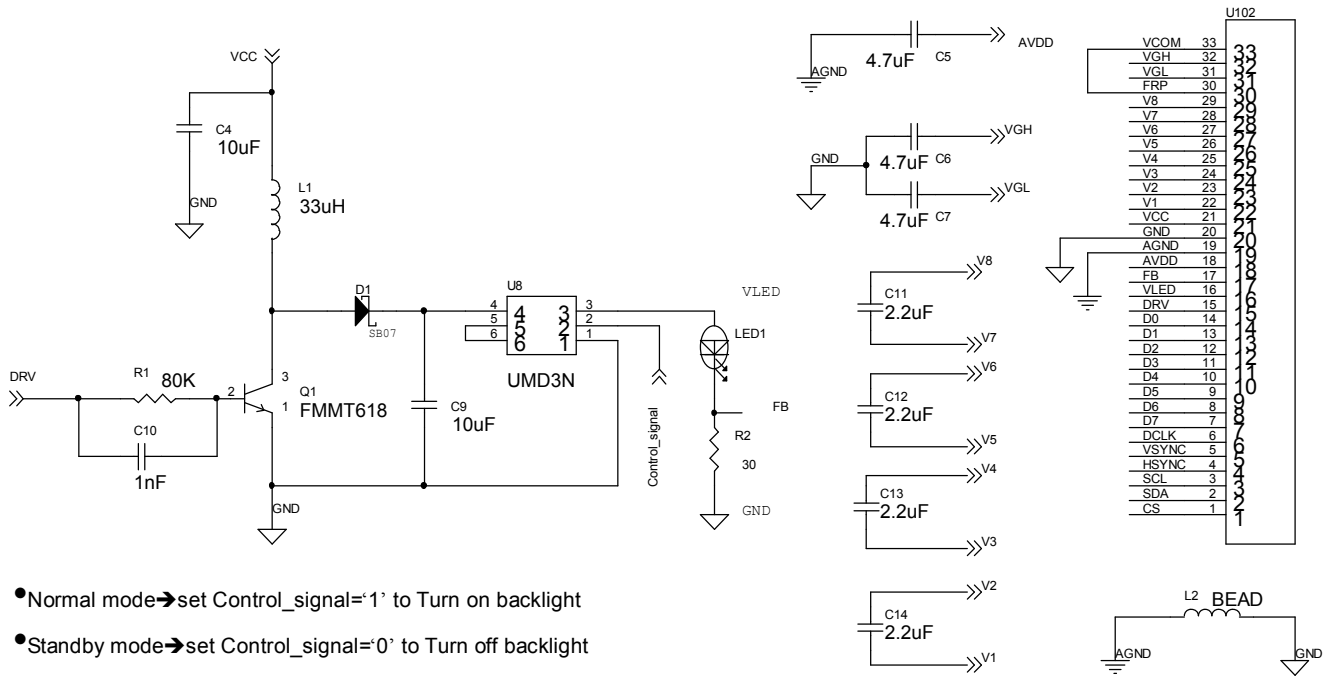
For UPS052 timing, there are three input RGB data modes to choose from: 320xRGB, 352xRGB, and 360xRGB. Input data is processed and mapped to display dots by integrated driver IC according to panel resolution and scan direction settings. UPS052 input format saves the effort of data scaling for users and keeps a consistent interface for different display resolutions, in the cost of higher input data rate and less image processing elasticity. An additional NTSC/PAL auto-detection function is provided for UPS052 input format. When the function is active, the HSYNC and VSYNC inputs are monitored. If there are more than 288 HSYNC in a VSYNC period, it is detected as the PAL mode (288 active lines). On the other hand, if there are less than 288 HSYNC in a VSYNC period, it is asserted as the NTSC mode (240 active lines). Please refer to the serial control setting for more details.

For vertical input timing, both UPS051 and UPS052 accept odd / even field switching or single field only input. For detail timing spec., please refer to Fig 2 and Fig 4.

2. Typical Application Circuit

a. Internal LED booster circuit

The integrated driver IC provides build-in LED booster controller, DC-DC charge pump, and Vcom driver. See Fig. 13 for the application circuit.



●Normal mode➔set Control_signal='1' to Turn on backlight

●Standby mode➔set Control_signal='0' to Turn off backlight

Fig.13 Typical Application Circuit

A single 3.3V power supply (VCC) is required to provide driver IC power and generate all necessary voltages for LCD related circuits.

According to Fig. 13, the L1, Q1, D1,and C9 together form the LED boost converter. The converter with 0.6V feedback (FB) and R2 provide a constant 20mA current for LED backlight unit. The boost converter switching signal DRV is generated base on divided frequency of DCLK. Therefore the DCLK input is required for LED driver operation, and the absent of DCLK signal during normal operation will set the driver IC into standby mode.UMD3N is a switch to control backlight ON/OFF,user should create a signal to control it. A low ESR capacitor for C9 is recommended in order to reduce voltage ripple of VLED. The build-in LED boost controller is default active, and it is able to be turned off by setting the register SHDB1 to low.

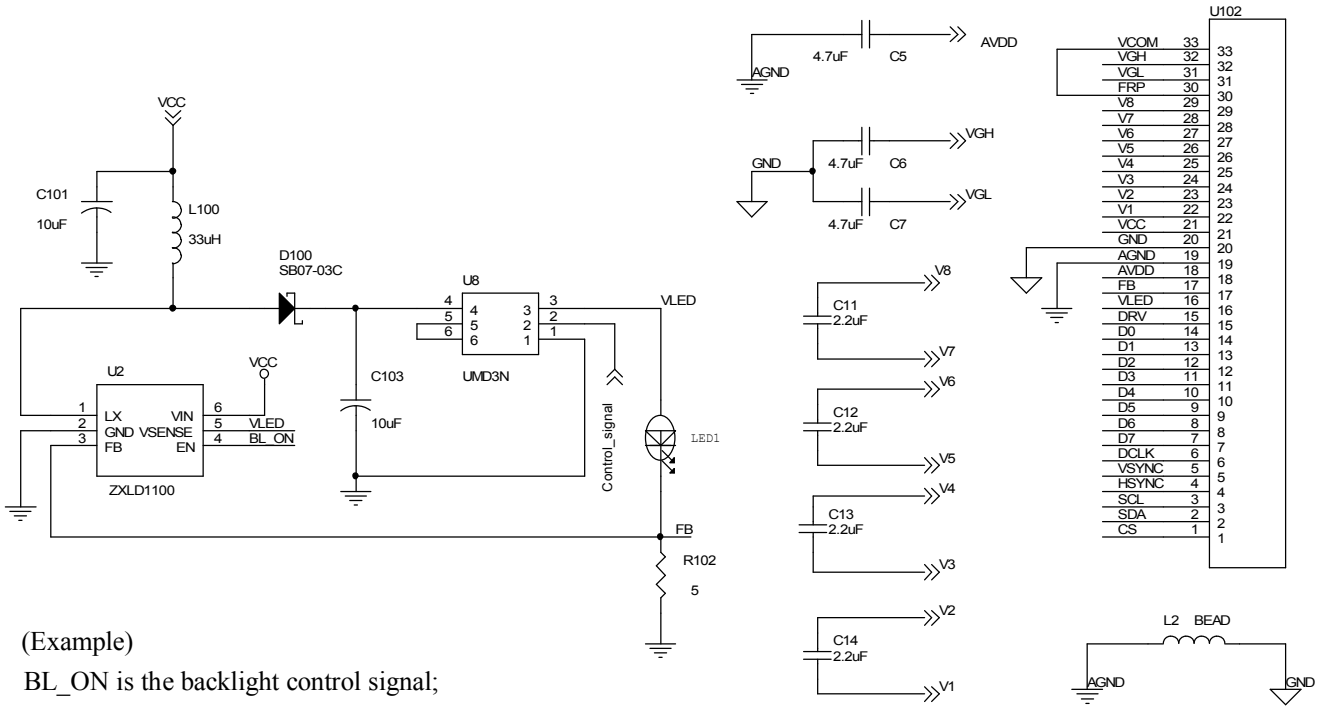
The positive (VGH) and negtive (VGL) power supplies for LCD are generated through build-in DC-DC charge pump circuit, an elegant design with only seven passive power-setting capacitors are required.

- PWM efficiency: about 75 ~ 80% (PWM_DUTY= "00")

The LED booster circuit may cause the wave like phenomenon, In order to reduce the phenomenon , AGND and DGND (system GND) and LED booster circuit GND must be separated. If the phenomenon is still seriously observed, use external LED driver circuit is the other way.

b. External LED driver circuit

Using external LED driver circuit is the best way to reduce the wave like phenomenon, Adopting external LED driver circuit is recommended , See Fig. 14 for the application circuit.



(Example)
BL_ON is the backlight control signal;
please refer to the power on/off sequence
of the product datasheet for recommended

Fig.14 External LED driver Circuit

Single 3.3V power supply (VCC) is required to provide driver IC power and generate all necessary voltages for LCD related circuits.

According to Fig. 14, the LED driver(ZXLD1100) and R102(5 ohm) with 0.1V feedback (FB) can provide a constant 20mA current for LED backlight unit. To control the back light on/off timing, user should create a control signal BL_ON (please refer to the ZXLD1100 date sheet). The LCD driver output DRV signal can also be used to drive BL_ON, in the condition of fine tune the R102 value to get the desired LED current value.

The build-in VCOM driver provides programmable amplitude and DC-level adjustments through serial control interface to optimize image contrast and minimize flicker. Optional external VCOM DC-level adjustment is achievable through external DC bias setting of FRP output (pin30) and VCOM input (pin33). The Fig. 15 is a simple external VCOM DC bias circuit for reference.

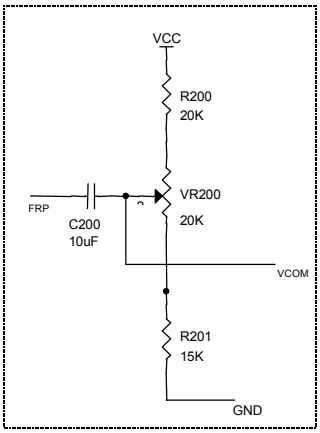


Fig.15 VCOM-DC External Adjustment Circuit

3. Power ON/OFF Sequence

After VCC power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VCC power-on, and setting register STB to high to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The driver IC analog power AVDD is turned on first, then the LCD negative power supply VGL is pumped, and then the LCD positive power supply VGH is pumped, and followed by the LED power VLED. Please refer to Fig.16 for the detail timing of power on/off sequence.

Since the LCD driver supports different panel resolutions, setting of output resolution is essential for proper LCD operation. The setting of output resolution is through register"PSL". For 1.5-inch 502x240 LCD: PSL[2:0] = 100. It is recommended to program essential serial commands first before releasing the LCD module from default standby mode. Please refer to Fig. 17 for recommend serial settings.

The DCLK signal is required for normal operation. When the DCLK is stopped for more than 5.6μsec (or DCLK frequency < 140KHz) during normal operation, the driver IC will be reset and operated in standby mode. This DCLK stop reset does not affect the serial interface settings.

4. Recommend scan direction settings

In order to prevent power on failure, the scan direction setting must be down-to-up and right-to-left when the TFT-LCD is power on. The recommended register setting sequence is as following:

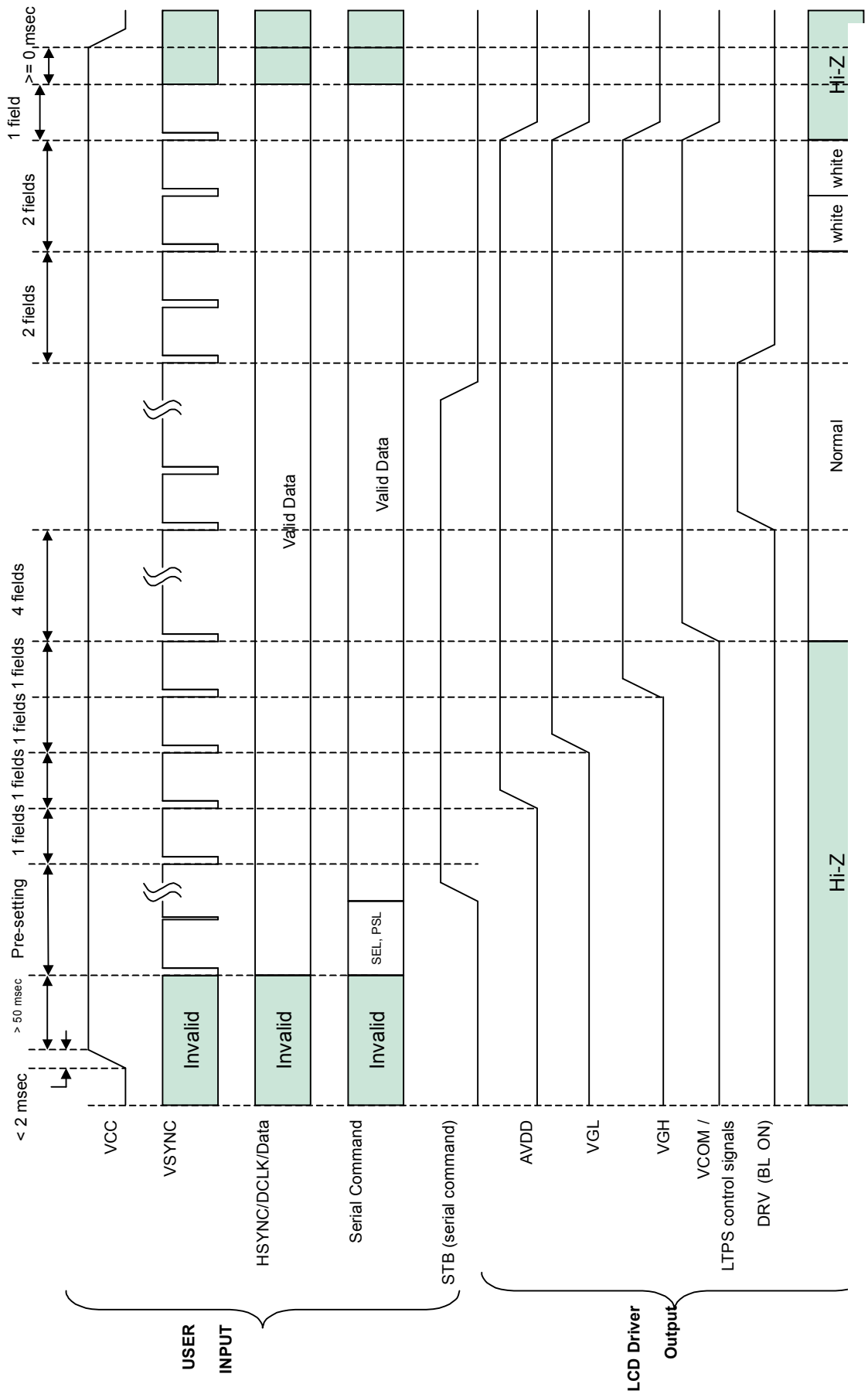
(1)Set the scan direction as down-to-up and right-to-left before standby releasing command.

(2)Send standby releasing command.

(3)Set the scan direction as up-to-down and left-to-right at least 1 field time after TFT-LCD starts to display.

(4)Turn on backlight for normal display.

Please refer to Fig 17 and Fig 18 for more details. This scan direction setting should be applied whenever the TFT-LCD is power on or the standby releasing command is send.



A. Fig.16 Power ON / OFF Sequence

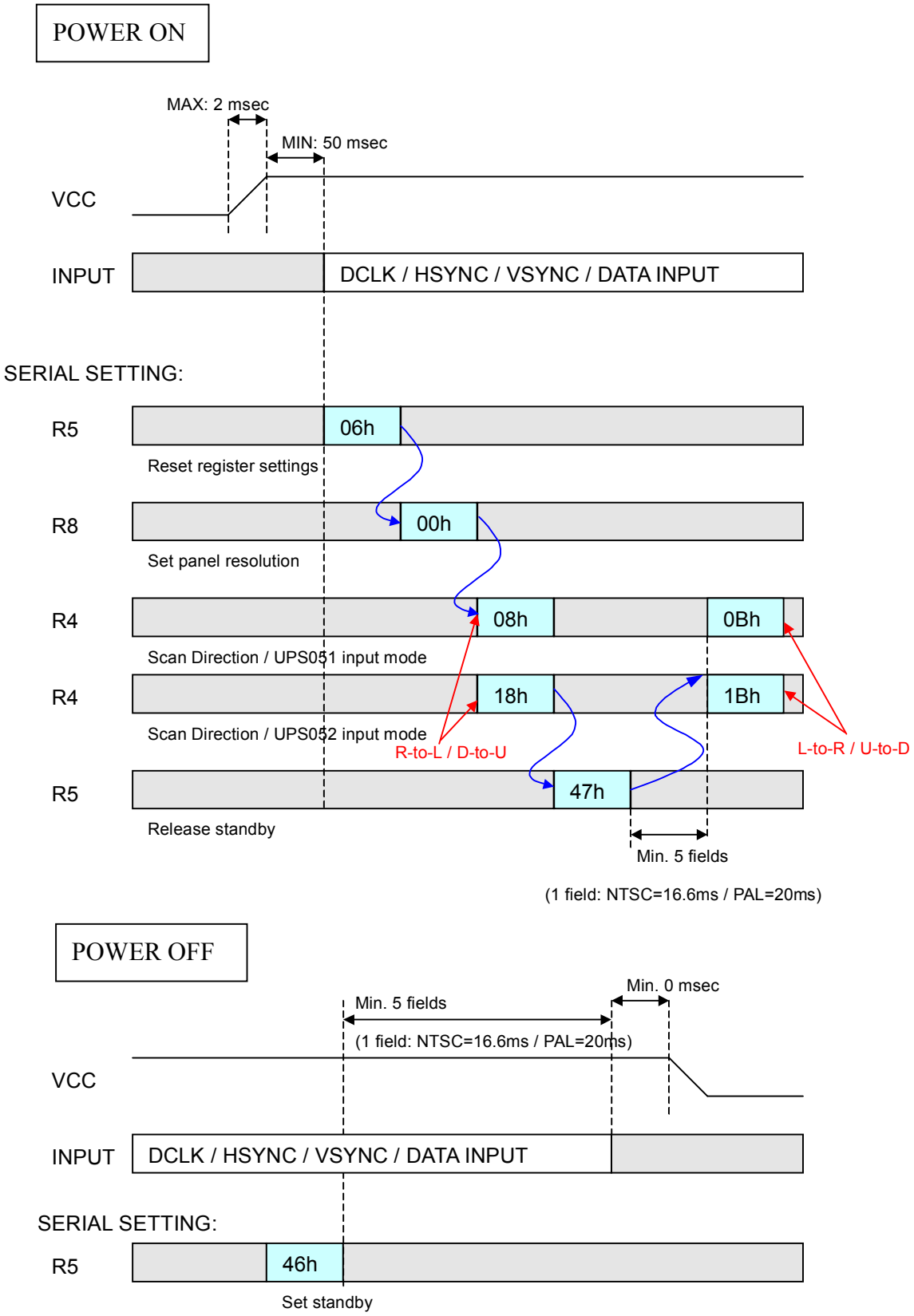


Fig 17. Recommend Serial Command Settings(1)

Standby Enable/Disable

SERIAL SETTING:

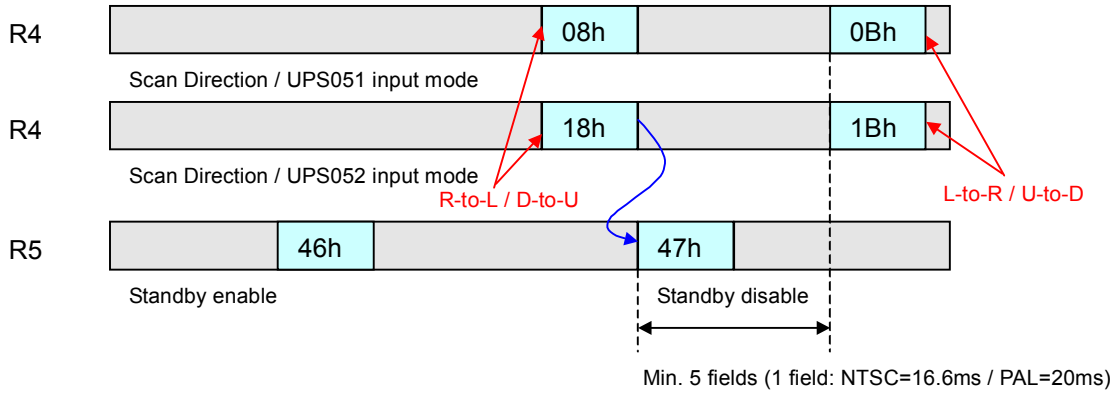


Fig 18. Recommend Serial Command Settings(2)